OPN7010

VCSEL Diode Driver Datasheet Rev1

FEATURES

- Support CMOS and LVDS input interface
- Up to 12V VSCEL supply voltage
- Up to 10A output current with configurable current limit
- Over current and over temperature detection and protection
- 12-bit ADC @ 1M/s sample rate
  - VCSEL diffuser-broken detection (PD/ITO) for eye protection
  - Output current sensing
  - Internal temperature monitoring
  - External temperature monitoring
- Smart correction for precision time control
- Support IO voltage 3.3V~5V
- Support I^2C interface

APPLICATIONS

- ToF camera illumination
- LIDAR illumination

PACKAGES

OPN7010Q

- 32-pin QFN
- 4mm × 4mm

GENERAL DESCRIPTION

The **OPN7010** is a smart VCSEL laser diode driver with high performance and high efficiency, which is optimized for Time of Flight (ToF) camera application. It is embedded with configurable current limit function to output specific peak current for illumination. A 12-bits ADC is also integrated for eye protection, temperature monitoring and output current sensing. The **OPN7010** supports I^2C interface configuration.

FUNCTION BLOCK DIAGRAM

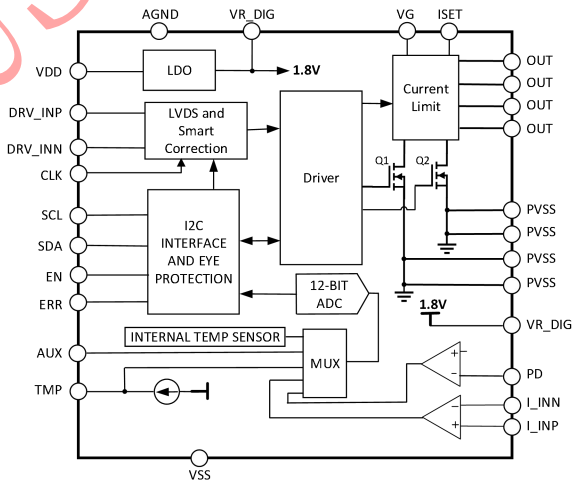


Figure 1. Block Diagram

PIN CONFIGURATION AND DESCRIPTION

Pin Configuration

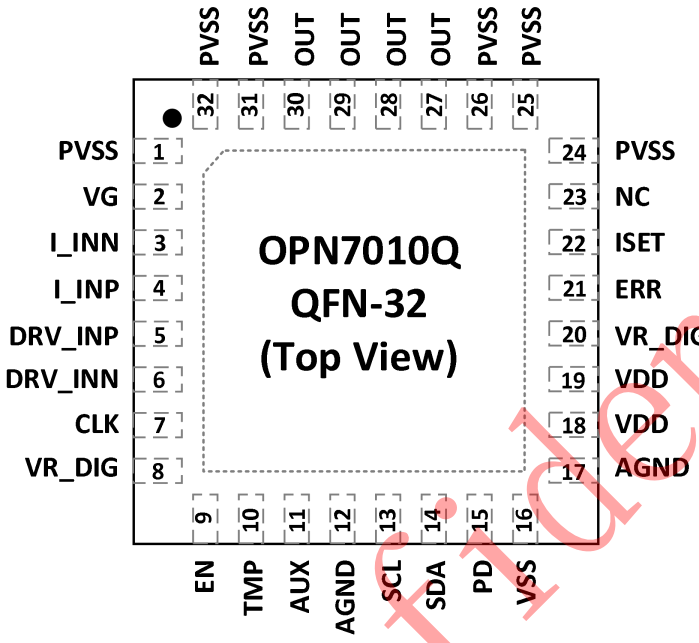


Figure.2 QFN Pin Configuration

Pin Description

QFN Pin	Pin Name	Description	Direction
1, 24, 25, 26, 31, 32	PVSS	Power Ground.	Ground
2	VG	Current Limit Gate Output.	AIO
3	I_INN	Current Sense Negative Input	AI
4	I_INP	Current Sense Positive Input	AI
5	DRV_INP	Driver Signal Positive Input.	DI
6	DRV_INN	Driver Signal Negative Input.	DI
7	CLK	Reference Clock Input.	DI
8, 20	VR_DIG	Internal LDO Output for Digital Circuit.	AO
9	EN	Driver Enable Pin.	DI
10	TMP	External Temperature Sensing Input. Connect a NTC resistor to AGND.	AI
11	AUX	AUX ADC Input.	AI
12, 17	AGND	Analog Ground.	Ground
13	SCL	I^2C Serial Clock. Require an external pull up resistor.	DI
14	SDA	I^2C Serial Data. Require an external pull up resistor.	DIO
15	PD	Photo Diode Sensing Input.	AI
16	VSS	Ground for internal circuit. Connect with AGND together.	Ground
18, 19	VDD	Internal Circuit Power Supply.	Power
21	ERR	ERROR Output or ADDR Select.	DIO
22	ISET	Current Limit Setting. Connect a resistor to AGND to set current limit level.	AI
23	NC	No Connect.	Floating
27, 28, 29, 30	OUT	Driver Output Node.	AO
	EPAD (Only QFN)	Exposed Pad(VSS). Connect with AGND together.	Ground

TYPICAL APPLICATION CIRCUIT

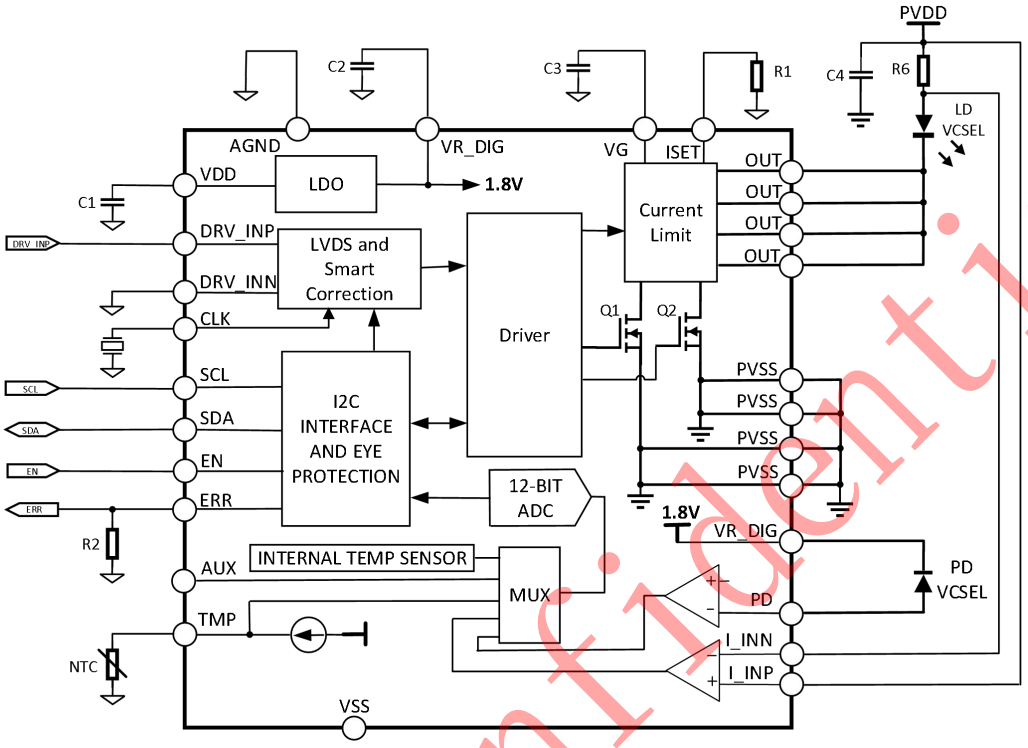


Figure 3. Typical application circuit (single-ended input)

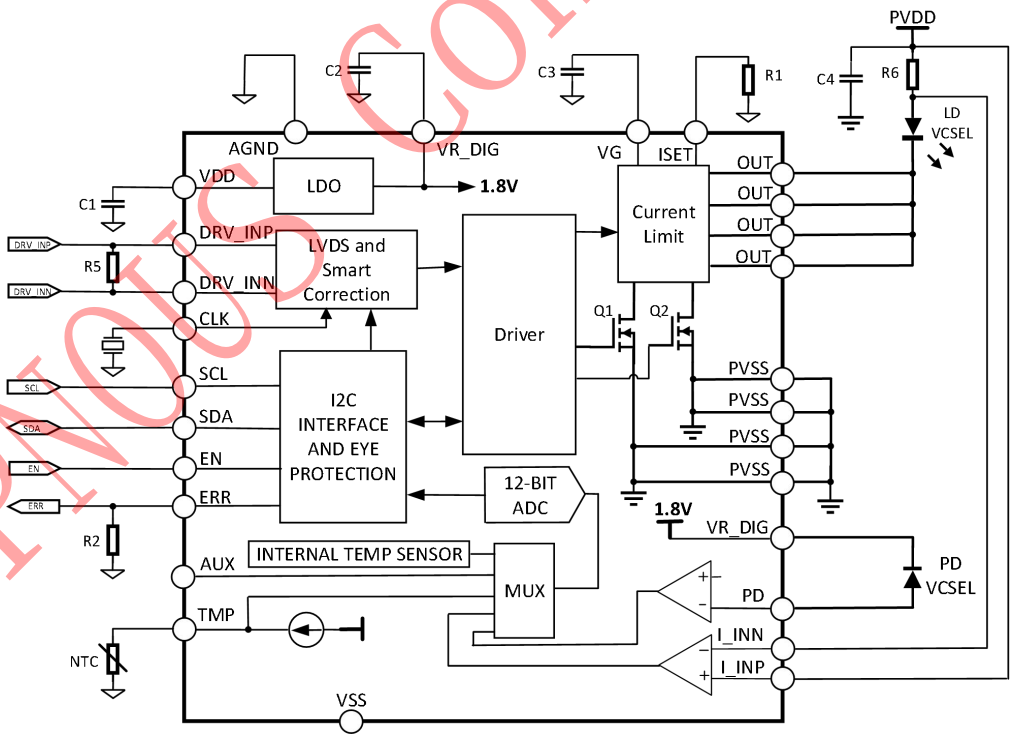
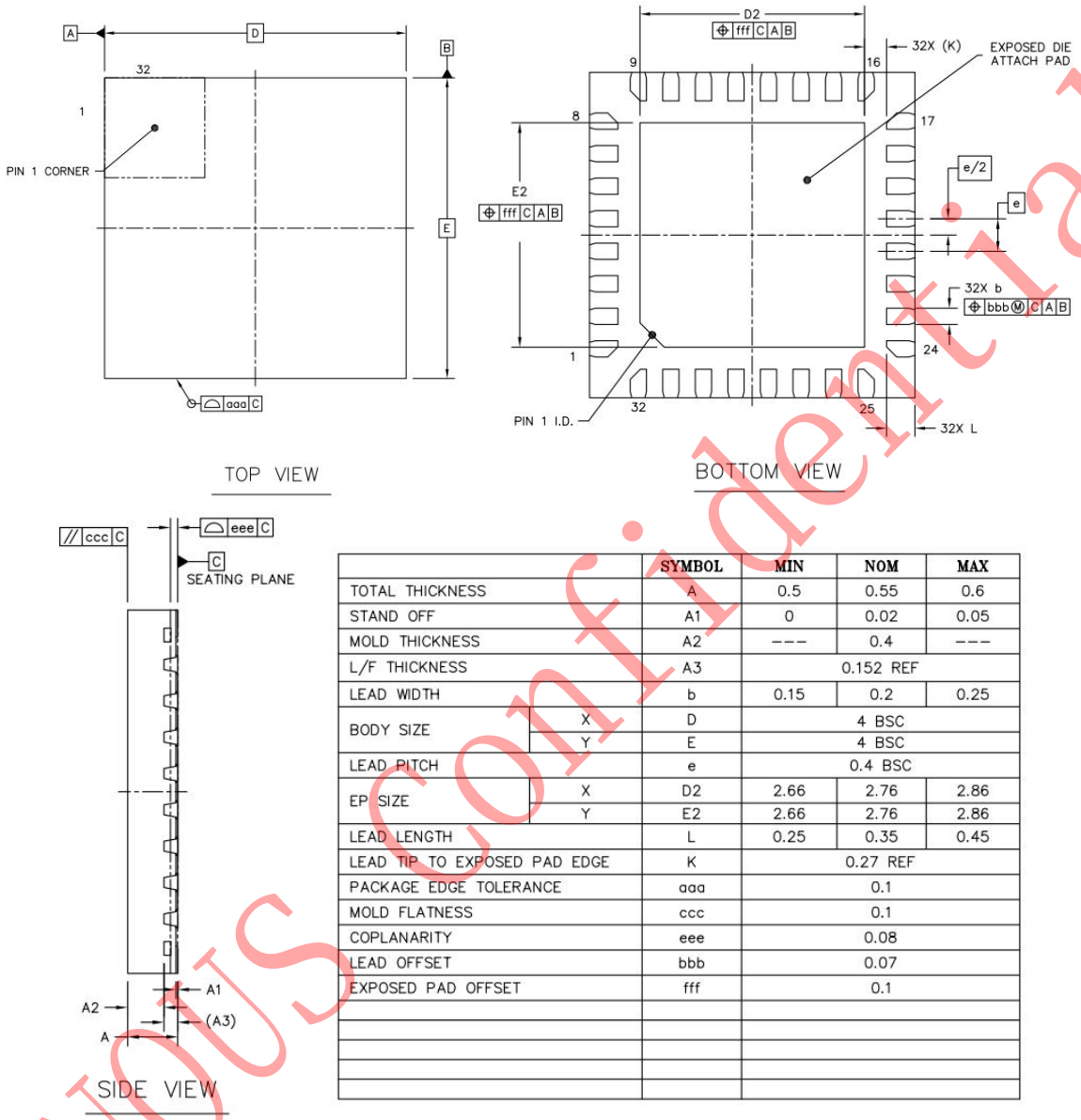


Figure 4. Typical application circuit (differential input)

PACKAGE OUTLINE DIMENSIONS



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	2.66	2.76	2.86
	Y	E2	2.66	2.76	2.86
LEAD LENGTH		L	0.25	0.35	0.45
LEAD TIP TO EXPOSED PAD EDGE		K		0.27 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

Figure 8. QFN Package Dimensions